

## CLAIMS

What is claimed is:

1. An apparatus, comprising:

charge storage circuitry to maintain a first amplitude of a first interrelated control signal and a second amplitude of a second interrelated control signal;

amplitude circuitry coupled to said charge storage circuitry to increase the first amplitude at a rate substantially equivalent to a rate of decrease in the second amplitude, to change an amplitude contribution of a reference clock phase, within high and low amplitude boundaries of a substantially small signal region of a transfer characteristic of phase control circuitry of a phase interpolator.

2. The apparatus of claim 1, further comprising common mode feedback circuitry coupled with said charge storage circuitry to maintain a substantially consistent common mode voltage between the first amplitude and the second amplitude.

3. The apparatus of claim 2, wherein the common mode feedback circuitry comprises

circuitry to compare the common mode voltage with a reference voltage;  
and

an output coupled to charge circuitry to increase the first amplitude and the second amplitude in response to the common mode voltage being less than the reference voltage, and coupled to discharge circuitry to decrease the first amplitude and the second amplitude in response to the common mode voltage being greater than the reference voltage.

- 1 4. The apparatus of claim 2, wherein the common mode feedback circuit comprises  
2 discrete time circuitry to output charging and discharging pulses for the first  
3 interrelated control signal and the second interrelated control signal.
- 1 5. The apparatus of claim 2, wherein the common mode feedback circuit comprises  
2 circuitry to facilitate a domination of an increase in the first amplitude over a  
3 decrease in the second amplitude.
- 1 6. The apparatus of claim 1, further comprising reference circuitry coupled with  
2 comparison circuitry to provide a high voltage boundary for the first amplitude  
3 and a low voltage boundary for the second amplitude.
- 1 7. The apparatus of claim 6, wherein the reference circuitry comprises a resistive  
2 ladder.
- 1 8. The apparatus of claim 6, wherein the reference circuitry further comprises a  
2 middle reference voltage to provide a reference for a common mode voltage  
3 between the first amplitude and the second amplitude.
- 1 9. The apparatus of claim 1, further comprising a leakage compensation circuit  
2 coupled with a capacitance circuit of said charge storage circuitry to compensate  
3 for differences in leakage of charge.
- 1 10. The apparatus of claim 9, wherein the leakage compensation circuit comprises an  
2 impedance to couple the capacitance circuit with a voltage supply node.
- 1 11. The apparatus of claim 1, wherein said charge storage circuitry comprises a  
2 capacitance circuit to provide a differential interrelated control signal for the  
3 reference clock phase.

1 12. The apparatus of claim 1, wherein said charge storage circuitry comprises a first  
2 capacitance circuit to store a first charge and a second capacitance circuit to store  
3 a second charge, wherein the first charge is substantially equivalent to the first  
4 amplitude and the second charge is substantially equivalent to the second  
5 amplitude.

1 13. The apparatus of claim 12, wherein said amplitude circuitry comprises a  
2 differential current-steering mechanism coupled to said charge storage circuitry to  
3 charge the first capacitance circuit and discharge the second capacitance circuit.

1 14. The apparatus of claim 1, wherein said amplitude circuitry comprises:  
2 charging circuitry to increase the first amplitude; and  
3 discharging circuitry to decrease the second amplitude in proportion to an  
4 increase in the first amplitude.

1 15. The apparatus of claim 1, wherein said amplitude circuitry comprises:  
2 trip high circuitry to compare the first amplitude to a high amplitude  
3 boundary; and  
4 trip low circuitry to compare the second amplitude to a low amplitude  
5 boundary.

1 16. The apparatus of claim 15, wherein said amplitude circuitry comprises:  
2 an overflow output to output an overflow signal in response to a charge  
3 stored by said charge storage circuitry; and  
4 hysteresis circuitry to prevent chatter in the overflow signal in response to  
5 the charge stored by said charge storage circuitry.

1 17. A method, comprising:

2 receiving a signal to transition a phase of an interpolated clock signal;  
3 increasing an amplitude of a first interrelated control signal in response to  
4 said receiving a signal, to increase an amplitude contribution of a  
5 first reference clock phase;  
6 decreasing an amplitude of a second interrelated control signal  
7 substantially simultaneously with said increasing an amplitude, to  
8 decrease an amplitude contribution of a second reference clock  
9 phase in proportion to the increase in the amplitude contribution of  
10 the first reference clock phase; and  
11 bounding the amplitudes of the first interrelated control signal and the  
12 second interrelated control signal between a high amplitude  
13 boundary and a low amplitude boundary, to change the phase of the  
14 interpolated clock signal with a substantially analog transition.

1 18. The method of claim 17, further comprising maintaining a common mode  
2 amplitude of the first interrelated control signal and the second interrelated control  
3 signal.

1 19. The method of claim 17, further comprising compensating for leakage of charge.

1 20. The method of claim 17, wherein said receiving a signal to transition the phase of  
2 the interpolated clock signal comprises receiving a signal to instruct charge  
3 circuitry to charge a first charge storage circuit associated with the first  
4 interrelated control signal and to discharge a second charge storage circuit  
5 associated with the second interrelated control signal.

1 21. The method of claim 17, wherein said increasing an amplitude comprises charging  
2 a first charge storage circuit to increase the amplitude contribution of the first  
3 reference clock phase.

1 22. The method of claim 17, wherein said decreasing an amplitude comprises  
2 discharging a second charge storage circuit to decrease the amplitude contribution  
3 of the second reference clock phase.

1 23. The method of claim 17, wherein said bounding the amplitudes comprises  
2 outputting an overflow signal to indicate that an amplitude of the amplitudes is  
3 substantially near at least one of the boundaries.

1 24. The method of claim 23, wherein outputting an overflow signal comprises  
2 outputting an overflow signal based on a hysteresis range of amplitudes to prevent  
3 chatter in the overflow signal.

1     25.     A system, comprising:  
2                circuitry to clock data with an interpolated clock signal;  
3                a phase interpolator to generate the interpolated clock signal based upon a  
4                first interrelated control signal and a second interrelated control  
5                signal; and  
6                a phase controller coupled to said phase interpolator, comprising  
7                charge storage circuitry to maintain a first amplitude of the first  
8                interrelated control signal and a second amplitude of the  
9                second interrelated control signal;  
10              amplitude circuitry coupled to said charge storage circuitry to  
11              increase the first amplitude at a rate substantially equivalent  
12              to a rate of decrease in the second amplitude, to change an  
13              amplitude contribution of a reference clock phase, within  
14              high and low amplitude boundaries of a substantially small  
15              signal region of a transfer characteristic of phase control  
16              circuitry of said phase interpolator.

1     26.     The system of claim 25, wherein the phase interpolator comprises a degenerative  
2                mesh to flatten a change in bias current associated with a change in the amplitude  
3                of the first interrelated control signal.

1     27.     The system of claim 25, wherein the amplitude circuitry comprises:  
2                charging circuitry to increase the first amplitude; and  
3                discharging circuitry to decrease the second amplitude in substantially  
4                inverse proportion to an increase in the first amplitude.

1 28. A machine-readable medium containing instructions, which when executed by a  
2 machine, cause said machine to perform operations, comprising:  
3 receiving a signal to transition a phase of an interpolated clock signal;  
4 increasing an amplitude of a first interrelated control signal in response to  
5 said receiving a signal, to increase an amplitude contribution of a  
6 first reference clock phase;  
7 decreasing an amplitude of a second interrelated control signal  
8 substantially simultaneously with said increasing an amplitude, to  
9 decrease an amplitude contribution of a second reference clock  
10 phase in proportion to the increase in the amplitude contribution of  
11 the first reference clock phase; and  
12 bounding the amplitudes of the first interrelated control signal and the  
13 second interrelated control signal between a high amplitude  
14 boundary and a low amplitude boundary, to change the phase of the  
15 interpolated clock signal with a substantially analog transition.

1 29. The machine-readable medium of claim 28, wherein said increasing an amplitude  
2 comprises charging a first charge storage circuit to increase the amplitude  
3 contribution of the first reference clock phase.

1 30. The machine-readable medium of claim 28, wherein said decreasing an amplitude  
2 comprises discharging a second charge storage circuit to decrease the amplitude  
3 contribution of the second reference clock phase.